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10/624,327	07/22/2003	Kyu-Mann Lee	5649-1136	7294

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,327	LEE ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-15,17-22,24-26 and 28-34* is/are rejected.

7)☒ Claim(s) *4,16,23,27 and 35-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/09/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In the Amendment dated December 20, 2004, claim **8** is canceled, and claims **1, 11, 12, 20 and 29-32** are amended are acknowledged. Accordingly, claims **1-7 and 9-38** are currently pending in this application.

Allowable Subject Matter

The indicated allowability of claims **8, 9, 11, 12 and 30-33** are withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Claim Objections

Claims **24 and 33** are objected to because of the following reasons.

In claim **24**, line 5, "pattering" should read –patterning--.

In claim **33**, "the ferroelectric layer is formed using a chemical solution deposition using a precursor of at least one of lead acetate[$Pb(CH3CO_2)_2$ $3H_2O$], zirconium n-butoxide [$Zr(n\text{-}OC_4H_9)_4$], and titanium isopropoxide [$Ti(i\text{-}OC_3H_7)_4$], and using a solvent 2-methoxyethano [$CH_3OCH_2CH_2OH$]" is not disclosed or described in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims **5 and 6** are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim **5** recites the limitation "the upper interlayer dielectric" in line 5. There is insufficient antecedent basis for this limitation in the claim **1**.

Claim **6** is rejected for incorporating the defects of the parent claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **1, 10, 13 and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by Koo (USP 5,959,879).

Regarding claims **1 and 10**, Koo discloses in Fig. 2 and corresponding texts as set forth in column 3, line 46-column 4, line 40, a ferroelectric memory device comprises:

a semiconductor substrate 100;

a lower interlayer dielectric 124 on the semiconductor substrate;

a plurality of ferroelectric capacitors formed of lower electrodes 110, ferroelectric films 114, and upper electrodes 116 on the lower interlayer dielectric; and

a plate line 118 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are substantially vertical relative to a top surface of the semiconductor substrate.

Regarding claim **13**, Koo discloses the ferroelectric pattern is at least one material from the group consisting of SrTiO3, $BaTiO_3$, $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $(Pb,La)(Zr,Ti)O_3$, and $Bi_4Ti_3O_{12}$ (col. 4, lines 8-11).

Regarding claim **20**, Koo discloses in Fig. 2 and corresponding texts as set forth in column 3, line 46-column 4, line 40, a method of fabricating a ferroelectric memory device comprises:

forming a lower interlayer dielectric 124 on a semiconductor substrate 100;

forming a plurality of ferroelectric capacitors formed of lower electrodes 110, ferroelectric films 114, and upper electrodes 116 on the lower interlayer dielectric; and

forming a plate line 118 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are substantially vertical relative to a top surface of the semiconductor substrate.

Claims **1, 7, 10, 13, 20 and 28** are rejected under 35 U.S.C. 102(e) as being anticipated by Ozaki (USP 6,521,929).

Regarding claims **1 and 10**, Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a ferroelectric memory device comprises:

a semiconductor substrate 1;

a lower interlayer dielectric 10 on the semiconductor substrate;

a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are substantially vertical relative to a top surface of the semiconductor substrate.

Regarding claim 7, Ozaki discloses in Fig. 1A the plurality of ferroelectric capacitors are arranged in rows and columns.

Regarding claim **13**, Ozaki discloses the ferroelectric pattern is at least one material from the group consisting of SrTiO3, $BaTiO_3$, $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $(Pb,La)(Zr,Ti)O_3$, and $Bi_4Ti_3O_{12}$ (col. 5, line 8).

Regarding claims **20 and 28**, Ozaki discloses in Figs. 1A-1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a method of fabricating a ferroelectric memory device comprises:

forming a lower interlayer dielectric 10 on a semiconductor substrate 1;

forming a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

forming a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein sidewalls of the ferroelectric capacitors are substantially vertical relative to a top surface of the semiconductor substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **2, 3, 21, 22, 24, 26, 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Figs 2-3 of Prior Arts and further in view of Evans, Jr. (USP 6,066,868).

Ozaki discloses the claimed limitations except for the device further comprises an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors; and hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric, and wherein the hydrogen barrier spacers are at least one from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2; the method further comprises forming hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric; and forming an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors; the method wherein forming the plate line comprises forming a lower plate layer on the semiconductor substrate and the hydrogen barrier spacers; and

patterning the lower plate layer/the metal wiring to form a plurality of parallel local plate lines, wherein each of the local plate lines directly contacts surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors; and wherein after forming the local plate line, the method further comprises sequentially forming a first upper interlayer dielectric layer and a second upper interlayer dielectric layer on the local plate lines. Figs 2-3 of Prior Arts disclose the device comprises an upper interlayer dielectric 33 on the lower interlayer dielectric 19 and the plurality of ferroelectric capacitors 32. Further, Figs 2-3 of Prior Arts teach the method comprises sequentially forming a first upper interlayer dielectric layer and a second upper interlayer dielectric layer on the lower interlayer dielectric layer. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors since it was known in the art that the upper interlayer dielectric formed on the lower interlayer dielectric is used to protect the plurality of ferroelectric capacitors. However, Figs 2-3 of Prior Arts fail to teach the device further comprises hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the lower interlayer dielectric. Evans teaches in Fig. 10 a memory cell 200 comprises hydrogen barrier spacers 225 between sidewalls of the ferroelectric capacitors and the silicon oxide layer 218, and the hydrogen barrier spacers are at least one from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2 (col. 6, lines 15-20). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form hydrogen barrier spacers between sidewalls of the ferroelectric capacitors and the silicon oxide layer and the hydrogen barrier spacers are at least one from the group consisting of TiO_2, Al_2O_3, ZrO_2, and CeO_2, as taught by Evans in order to inhibit the flow of oxygen to the top and bottom electrodes

when the memory cell is placed in a gaseous environment containing hydrogen (col. 3, lines 43-47).

Claims **9, 15, 17-19 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Figs 2-3 of Prior Arts.

Regarding claims **9 and 29**, Ozaki discloses the claimed limitations except for sidewalls of the ferroelectric capacitors have an inclination of about 70° to about 90° relative to a top surface of the semiconductor substrate. Figs 2-3 of Prior Arts disclose that the ferroelectric capacitors 32 have sloped sidewalls. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form sidewalls of the ferroelectric capacitors having an inclination of about 70° to about 90° relative to a top surface of the semiconductor substrate, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim **15**, Ozaki discloses in Fig. 1B the plate line is a local plate line directly contacting the surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors except for the device further comprises an upper interlayer dielectric covering the local plate line. Figs 2-3 of Prior Arts disclose that the device comprises an upper interlayer dielectric 33 covering the plurality of ferroelectric capacitors 32. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors to cover the plate line to protect the plurality of ferroelectric capacitors and the plate line.

Regarding claims **17-18**, Ozaki discloses the claimed limitations except for the device further comprises an insulation pattern between the plate line and the lower interlayer dielectric, and wherein the insulation pattern is an upper interlayer dielectric. Figs 2-3 of Prior Arts disclose that the device comprises an upper interlayer dielectric 33 covering the plurality of ferroelectric capacitors 32. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors to cover the plate line to form an insulation pattern between the plate line and the lower interlayer dielectric to protect the plurality of ferroelectric capacitors and the plate line.

Regarding claim **19**, Ozaki discloses the claimed limitations except for the device further comprises an upper interlayer dielectric on the plurality of ferroelectric capacitors, and main word lines on the upper interlayer dielectric. Figs 2-3 of Prior Arts disclose that the device comprises an upper interlayer dielectric 33 covering the plurality of ferroelectric capacitors 32, and main word lines 35 on the upper interlayer dielectric. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form an upper interlayer dielectric on the lower interlayer dielectric and the plurality of ferroelectric capacitors to cover and to protect the plurality of ferroelectric capacitors, and to include main word lines to control gate electrodes (see Background of Invention).

Claims **11 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Mikawa et al. (USP 6,602,721 hereinafter referred to as "Mikawa").

Regarding claim **11**, Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a ferroelectric memory device comprises:

a semiconductor substrate 1;

a lower interlayer dielectric 10 on the semiconductor substrate;

a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

Ozaki fails to teach the lower and upper electrodes comprise at least one of ruthenium and ruthenium oxide. Mikawa teaches in Fig. 1 a ferroelectric memory device comprises the lower electrode 15 and the upper electrode 18 comprising at least one of ruthenium and ruthenium oxide (col. 6, lines 55-61). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the lower electrode and the upper electrode comprising at least one of ruthenium and ruthenium oxide, as taught by Mikawa in order for the electrodes, even if a high-temperature heat treatment is performed with respect to the capacitor insulating film composed of a ferroelectric material, which is a metal oxide, to be stable and less reactive with oxygen contained in the metal oxide as set forth in column 8, lines 58-65).

Regarding claim **30**, Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a method of fabricating a ferroelectric memory device comprises:

forming a lower interlayer dielectric 10 on a semiconductor substrates 1;

forming a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

forming a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer 5a, a ferroelectric layer 6, and an upper electrode 7a laver on the lower interlayer dielectric; and

successivelv patterning the upper electrode layer, the ferroelectric laver, and the lower electrode laver to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions.

Ozaki fails to teach the lower electrode layer and the upper electrode layer are formed from at least one of ruthenium and ruthenium oxides. Mikawa teaches in Fig. 1 a ferroelectric memory device comprises the lower electrode 15 and the upper electrode 18 comprising at least one of ruthenium and ruthenium oxide (col. 6, lines 55-61). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the lower electrode and the upper electrode comprising at least one of ruthenium and ruthenium oxide, as taught by Mikawa in order for the electrodes, even if a high-temperature heat treatment is performed with respect to the capacitor insulating film composed of a ferroelectric material, which is a metal oxide, to be stable and less reactive with oxygen contained in the metal oxide as set forth in column 8, lines 58-65).

Claims **12 and 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Kim et al. (USP 6,229,166 hereinafter referred to as "Kim").

Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a ferroelectric memory device comprises:

a semiconductor substrate 1;

a lower interlayer dielectric 10 on the semiconductor substrate;

a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors.

Ozaki fails to teach the ferroelectric pattern comprises PZT(Pb,Zr,TiO_3) with $PbTiO_3$ as a seed layer. Kim teaches in Fig. 1 the ferroelectric layer 116 using PZT, the upper and lower seed layers 114 and 118 are preferably formed using $PbTiO_3$ as set forth in column 4, lines 40-42. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the ferroelectric layer using PZT, the upper and lower seed layers and are preferably formed using $PbTiO_3$, as taught by Kim in order to improve ferroelectric capacitor characteristics as set forth in the Abstract.

Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Yamoto et al. (USP 6,355,952 hereinafter referred to as "Yamoto").

Ozaki discloses the claimed limitations except for the plate line is at least one material from the group consisting of the platinum group including ruthenium, platinum, iridium,

rhodium, Osmium, and palladium, and oxides thereof. However, Yamoto teaches in Fig. 8E that a capacitor comprises a plate line 42 may be composed of platinum (col. 16, line 29). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the plate line composed of platinum, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claim **25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Figs 2-3 of Prior Arts and further in view of Evans, Jr. (USP 6,066,868) and Mikawa et al. (USP 6,602,721 hereinafter referred to as "Mikawa").

Ozaki, Figs 2-3 of Prior Arts and Evans discloses the all claimed limitations except for the method wherein prior to the forming the lower plate line, the method further comprises: forming an insulation layer on the semiconductor substrate and the hydrogen barrier spacers; and planarizing the insulation layer until surfaces of the ferroelectric capacitors are exposed, and leaving an insulation pattern tilling a gap region between the ferroelectric capacitors. Mikawa teaches in Figs. 9C and 10A a method for fabricating a ferroelectric memory device comprises the burying-insulating-film forming film 16A composed of a silicon dioxide, a silicon nitride, or the like is deposited over entire surface of the interlayer insulating film 13 including the lower electrodes 22 and the protective films 23. Next, the planarizing step is performed by CMP with respect to the burying-insulating-film forming film till the lower electrodes 15 are exposed, thereby forming the burying insulating film 16 from the burying-insulating-film forming film (col. 12, lines 17-27). It would have been obvious to one of ordinary skill in the art at the time

of the invention was made to utilize the Mikawa's teaching for the method wherein prior to the forming the lower plate line, forming an insulation layer on the semiconductor substrate and the hydrogen barrier spacers; and planarizing the insulation layer until surfaces of the ferroelectric capacitors are exposed, and leaving an insulation pattern tilling a gap region between the ferroelectric capacitors to prevent the formation of a recess (col. 12, lines 43-44).

Claim **31** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Chang et al. (USP 6,638,441 hereinafter referred to as "Chang").

Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a method of fabricating a ferroelectric memory device comprises:

forming a lower interlayer dielectric 10 on a semiconductor substrates 1;

forming a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

forming a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer 5a, a ferroelectric layer 6, and an upper electrode 7a laver on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric laver, and the lower electrode laver to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions.

Ozaki fails to teach successively patterning the upper electrode layer, the ferroelectric capacitor layer, and the lower electrode layer comprises anisotropically etching using a plasma containing oxygen. Chang teaches that anisotropically etching using a plasma containing oxygen is used to etch and remove layers in a method for pitch reduction. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of anisotropically etching using a plasma containing oxygen, as taught by Change in order to form various device structures with a tiny dimension (col. 4, lines 18-20).

Claim **33** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USP 6,521,929) in view of Gilbert et al. (USP 6,730,354 hereinafter referred to as "Gilbert").

Ozaki discloses in Fig. 1B and corresponding texts as set forth in column 4, line 23-column 5, line 62, a method of fabricating a ferroelectric memory device comprises:

forming a lower interlayer dielectric 10 on a semiconductor substrates 1;

forming a plurality of ferroelectric capacitors formed of lower electrodes 5a, ferroelectric films 6, and upper electrodes 7a on the lower interlayer dielectric; and

forming a plate line/a metal wiring 9 that extends across and electrically connects to surfaces of at least two adjacent ones of the plurality of ferroelectric capacitors, wherein forming a plurality of ferroelectric capacitors comprises:

sequentially forming a lower electrode layer 5a, a ferroelectric layer 6, and an upper electrode 7a laver on the lower interlayer dielectric; and

successively patterning the upper electrode layer, the ferroelectric laver, and the lower electrode laver to form a plurality of stacked lower electrode, ferroelectric pattern, and upper electrode structures that are arranged in row and column directions.

Ozaki fails to teach the ferroelectric layer is formed using a chemical solution deposition using a precursor of at least one of lead acetate[$Pb(CH3CO_2)_2$ $3H_2O$], zirconium n-butoxide [$Zr(n\text{-}OC_4H_9)_4$], and titanium isopropoxide [$Ti(i\text{-}OC_3H_7)_4$], and using a solvent 2-methoxyethano [$CH_3OCH_2CH_2OH$]. Gilbert teaches that in improved methods of forming PZT thin films, a source reagent solution comprises a mixture of a lead precursor, a titanium precursor and a zirconium precursor in a solvent medium is provided (col. 2, line 54-col. 3, line 59). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of a source reagent solution comprises a mixture of a lead precursor, a titanium precursor and a zirconium precursor in a solvent medium is provided in the methods of forming PZT thin films, as taught by Gilbert in order for the PZT thin films having thickness of 70 nm or less to be fabricated with high within-wafer uniformity, high throughput and at a relatively low temperature (col. 2, lines 54-59).

Allowable Subject Matter

Claims **4, 16, 23, 27 and 35-38** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ozaki, Yamoto, Evans, Kim, Koo, Mikawa, Chang, Gilbert, Yamoto and Figs 2-3 of Prior Arts, taken

alone or in combination, fail to teach the claimed invention the device wherein the plate line covers sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric as recited in claim **4**; the device wherein the plate line is a main plate line directly contacting the surfaces of the at least two adjacent ones of the plurality of ferroelectric capacitors via a slit-type via hole penetrating the upper interlayer dielectric as recited in claim **16**; the method wherein the forming a plate line comprises forming the plate line on sidewalls of the hydrogen barrier spacers and a surface of the lower interlayer dielectric as recited in claim **23**; the method further comprises successively patterning the second and first interlayer dielectric layers to form a slit-type via hole exposing a portion of the local plate lines; and forming a main plate line covering the slit-type via hole as recited in claim **27**; and the method wherein forming the upper interlayer dielectric and the forming the plate line comprises successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing a surface of the ferroelectric capacitor in a row direction, and forming a main plate line covering the slit-type via hole as recited in claim **35**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

02/09/05

Andy Huynh

Patent Examiner